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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,611	07/07/2005	Satoshi Yamanaka	0925-0220PUS1	8340

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EXAMINER	
ZHU, RICHARD Z	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
08/14/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/541,611	YAMANAKA ET AL.	
	Examiner	Art Unit	
	RICHARD Z. ZHU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/04/2009 has been entered.

Response to Applicant's Arguments

2. Applicant's arguments in view of the amendment are persuasive. As such, previous grounds of rejection under ***Zhang*** are withdrawn. Upon further search, the examiner is entering new grounds of rejections on the basis of ***Maenaka et al (US 7039254 B1)***.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 USC 103(a) as being unpatentable over ***Maenaka et al (US 7039254 B1)*** in view of ***Jiang (US 7242819 B2)***.

Regarding the apparatus of Claim 1 and therefore method of Claim 4, *Maenaka* discloses a pixel interpolation circuit **(Figs 7 or 8)** for generating interpolation pixel data which interpolates an input image based on pixel data composing the input image **(Figs 7 or 8, original image data from memory unit)**, the pixel interpolation circuit comprising:

an interpolation unit **(Fig 7 and see Col 15, Rows 38-45, Correlation Value Operating Unit 2)** for calculating interpolation candidate data of the same interpolation pixel **(Col 12, Rows 6-13 and Rows 38-48, calculating a range S from which candidate pixel data for interpolated pixel X can be found)** based on calculations performed on test interpolation data of a plurality of normal pixels neighboring the interpolation pixel **(Fig 6 and see Col 12, Rows 38-48)**, where each interpolation candidate data is to be interpolated using different interpolation methods **(Fig 1 and see Col 12, Row 52 – Col 13, Row 22, interpolation methods D11-D23, D12-D22, and D13-D21)**;

a determining circuit **(Fig 7, Correlation Operating Unit 2, Minimum Extracting Unit 3, and Pixel Data Selecting Unit 4. See Col 15, Rows 40-54)** for selecting one of the interpolation circuits based on a difference between the test interpolation data and actual

pixel data of said plurality of normal pixels (**Pixel data selecting unit selects base on outputs of minimum extracting unit where a "High" flag control signal is generated for the smallest one of L1-L3 and R1-R3, see Col 16, Rows 58-65; wherein L1 through R3 are difference between test interpolation data x and actual pixel data d11-d27 of Fig 6. Note that d11-d27 are 8 bit pixel data with values between 0 and 255 and x is set from range S defined by d11-d27, see Col 11, Rows 47-55 and Col 12, Rows 18-37 respectively**); and

an output circuit for outputting the interpolation candidate data calculated by the selected interpolation circuit as the interpolation pixel data (**Fig 7, Average Operating Unit 6 and see Col 15, Rows 55-61**).

While ***Maenaka*** interpolation unit independently calculates interpolation candidate data of the same interpolation pixel using respective different interpolation methods, ***Maenaka*** does not disclose the internal structure of said unit comprise a plurality of independent interpolation circuits.

Jiang discloses a very similar interpolation circuitry that takes edge direction into consideration when performing interpolation (**See Figs 1-2**) having an internal structure comprising a plurality of interpolation circuits with specific logic components each independently calculates interpolation candidate data (**Fig 8, Adder Logic 88 and Division Logic 90**) of a same pixel to be interpolated (**Fig 1, Pixel to be interpolated**), using different interpolation methods (**Col 13, Rows 48-58**).

Jiang demonstrated that it is well known in the art to implement separate sets of logic to form independent circuits to each perform its respective interpolation methods, it would've

been obvious to one of ordinary skill in the art at the time of the invention to design the internal circuitry of ***Maenaka***'s interpolation unit with independent circuits to calculate respective correlation values of respective different interpolation methods such that its intended function as disclosed would be successfully implemented.

Regarding Claims 2 and 5, ***Maenaka*** discloses wherein the determining circuit calculates a evaluation data for each of the interpolation circuits, by summing up the absolute values of the difference between the test interpolation data and the actual pixel data, and selects one of the interpolation circuits based on the evaluation data **(See for example Col 12, Row 60 and Col 13, Row 5, d11, d13, d21, and d23 are actual pixel data, x is test interpolation data chosen from candidate pixel data defined by range S. Therefore, correlation value L or evaluation data is the summation of absolute values of difference between actual pixel data d11-d23 and test interpolation data x. The minimum of L calculated from every value from range S is chosen to be Lmin)**.

Regarding Claims 3 and 6, ***Maenaka*** discloses wherein the determining circuit calculates binarized or ternarized values of the difference between the test interpolation data and the actual pixel data **(Col 16, Rows 35-44, at least two and more sets of neighboring pixels are chosen for relevant calculation)**.

5. Claim 7 is rejected under 35 USC 103(a) as being unpatentable over ***Maenaka et al (US 7039254 B1)*** and ***Jiang (US 7242819 B2)*** in view of ***Utagawa (US 6563538 B1)***.

Regarding Claim 7, ***Maenaka*** does not disclose a scanner employing said interpolation circuits. ***Utagawa*** discloses an image scanner comprising an image scanner comprising a pixel interpolation circuit (**Fig 2 and see Col 5, Rows 32-40**).

Since it is well known in the art that scanner employs interpolation circuits, it would've been obvious to one of ordinary skill in the art at the time of the invention to implement ***Maenaka***'s circuit for ***Utagawa***'s scanner such that edge pixels can be properly interpolated in view of the advantages offered by ***Maenaka***.

Conclusion

6. Additional Prior arts of record to be consider:

   - ***Suga et al (US 5832143 A)*** discloses a method for choosing the optimal interpolation method on the basis of pixel data difference between interpolated pixel and each of the actual pixels around the interpolated pixel.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Richard Z. Zhu whose telephone number is 571-270-1587 or examiner's supervisor King Y. Poon whose telephone number is 571-272-7440. Examiner Richard Zhu can normally be reached on Monday through Thursday, 0630 - 1700.

   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RZ^2
07/09/2009

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